UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,969	09/22/2003	Katsumi Abe	q75817	4962

23373 7590 07/17/2008

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
PHAM, TAMMY T	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
07/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,969	ABE, KATSUMI	
	Examiner	Art Unit	
	TAMMY PHAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 29-35* is/are pending in the application.

4a) Of the above claim(s) *8-15 and 22-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,16-21 and 29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 27-28 have been cancelled. Claims 8-15, 22-26 have been withdrawn. Claims 33-35 have been added. Claims 1-7, 16-21, 29-35 are considered below.

Response to Arguments

2. Applicant's arguments filed 2 April 2008 have been fully considered but they are not persuasive.

3. § 102 Rejection

4. **In regards to independent claim 1,** Applicant submits that *"the capacitor C1 and VDD are both connected directly or indirectly to the source terminal of TR3 (Remarks 20)."* This is not persuasive.

5. The claim language still remains broad. In particular, the claim language currently states of *"at least one capacitance load connected to respective terminals of the first and the second transistors not connected to the first and second voltage supplies (claim 1, lines 11-12)."* The claim language as currently stated fails to specify that the capacitance load is not indirectly connected to the first and second voltage supplies.

6. Akiyama teaches of at least one capacitance load (Drawing 6, items C1, C2) connected to respective terminals of the first (Drawing 6, items TR1, TR3) and the second transistors (Drawing 6, items TR2, TR4) not connected to the first (Drawing 6, item Vdd) and second

voltage supplies (Drawing 6, item Vee). Hence, Akiyama continues to read upon the claim language as currently stated.

7. **In regards to independent claim 1,** Applicant further submits that *"VCOM alleged to be the at least one signal line is connected to the drains of transistors TR3 and TR4 (Remarks 21)."* This is not persuasive.

8. The claim language still remains broad. The claim language as currently stated fails to specify that the signal line is directly connected to each gate terminal. Hence, Akiyama continues to read upon the claim language as currently stated.

9. **In regards to independent claim 1,** Applicant further submits that *"there is no disclosure of a high level of signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply and a low level signal passing through the signal line is lower than the low level voltage signal supplied by the second voltage supply (Remarks 21)."* This is not persuasive.

10. The claim language still remains broad. Akiyama teaches that the high level of signal (Fig. 6, item +Vdd) passing through the at least one signal line (Fig. 6, item Vcom) is higher than the high level voltage signal supplied by the first voltage supply (Fig. 6, item –Vee) and that the low level signal (Fig. 6, item –Vee) passing through the signal line (Fig. 6, item Vcom) is lower than the low level voltage signal supplied by the second voltage supply (Fig. 6, item +Vdd).

11. **In regards to claim 6,** Applicant submits that *"Akiyama fails to disclose that the transistor provided in VCOM driver circuit is TFT (Remarks 21-22)."* This is not persuasive. Akiyama teaches that the first and second transistors are comprised of thin-film transistors (section [0012]).

12. **In regards to claim 29,** Applicant submits that *"Akiyama does not disclose a level shift circuit connected to the one signal line directly or via a buffer circuit (Remarks 22)."* This is not persuasive. Akiyama teaches of a level shift circuit (Fig. 2, item 12, section [0014]) connected to one signal line (Fig. 2, items X1-X64x3) directly.

13. § 103 Rejection

14. **In regards to claim 2, 16,** Applicant submits that it would not have been obvious to place the common drive circuit of Akiyama in the particular order as taught by Hosokawa (Remarks 22-25). This is not persuasive.

15. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one having ordinary skill in the art to have the common drive circuit be positioned position to the gate driver circuit with the display portion in

between as taught by Hosokawa with the common drive circuit of Akiyama, since the repositioning of these elements is in no way critically dependent upon the overall operation of the display, and further this configuration could be combined to achieve the predictable result of space and cost efficiency when a display is located in a compact area.

16. **In regards to claims 2, 16,** Applicant further submits that *"Examiner does not indicate how cost and space efficiency occurs when a display is located between a gate driver and a common drive circuit (Remarks 24)."* This is not persuasive.

17. In response to applicant's argument that the examiner's conclusion of obviousness is based upon insufficient explanation or indication, it must be emphasized that an invention that would have been obvious to a person of ordinary skill at the time of the invention is not patentable. See *KSR v. Teleflex,* 127 S. Ct. 1727, 82 U.S.P.Q. 2d 1385 (2007). In this particular case, it would have been obvious to one with ordinary skills in the art to recognize that (1) the way known elements are arranged (such as the gate and common driver of a display) takes up a certain amount of space; and (2) that by rearranging the known elements in a certain way, one can maximize on space efficiency.

Information Disclosure Statement

18. The information disclosure statement (IDS) submitted on 9 April 2008 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claim 1, 3, 6-7, 29, 33, 35, are rejected under 35 U.S.C. 102(b) as being anticipated by Akiyama et al. (Japanese Publication No: 11-194316).

20. **As for independent claims 1, 33,** Akiyama teaches of a common drive circuit (Drawing 6) for a display (Drawing 2, item 10), the common drive circuit (Drawing 6) comprising:

21. a first voltage supply (Drawing 6, item +Vdd) and a second voltage supply (Drawing 6, item –Vee) which respectively supply a high level voltage signal (Drawing 6, item +Vdd) and a low level voltage signal (Drawing 6, item –Vee) to a common electrode;

22. at least one first transistor (Drawing 6, items TR1, TR3) including either a drain or a source terminal connected to the first voltage supply (Drawing 6, item +Vdd);

23. at least one second transistor (Drawing 6, items TR2, TR4) including either a drain or source terminal connected to the second voltage supply (Drawing 6, item –Vee);

24. at least one signal line (Drawing 6, item VCOM) connected to each gate terminal of the first (Drawing 6, items TR1, TR3) and second transistor (Drawing 6, items TR2, TR4); and

25. at least one capacitance load (Drawing 6, items C1, C2) connected to respective terminals of the first (Drawing 6, items TR1, TR3) and the second transistors (Drawing 6, items TR2, TR4) not connected to the first (Drawing 6, item +Vdd) and second voltage supplies (Drawing 6, item -Vee),

26. wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply (Drawing 6, item +Vdd) and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by the second voltage supply (Drawing 6, item –Vee, section [0047]).

27. **As for claim 3,** Akiyama teaches that at least one first transistor comprises P-type transistor (Drawing 6, items TR1, TR3, section [0018]) and the at least one second transistors comprises N-type transistor (Drawing 6, items TR2, TR4, section [0019]), and

28. wherein the gate terminals of the first and second transistors are connected to common signal lines (Drawing 6, items VCOM).

29. **As for claim 6,** Akiyama teaches that the first (Drawing 6, items TR1, TR3) and second transistors (Drawing 6, items TR2, TR4, section [0018]) are comprised of thin-film transistors.

30. **As for claim 7,** Akiyama teaches that the display portion comprises a liquid crystal display (Drawing 2, item 10, section [0002]).

31. **As for claim 29,** Akiyama teaches that of a level shift circuit (Drawing 2, item 12, section [0014]) connected to the one signal line (Drawing 2, items X1-X640x3) directly.

32. **As for claim 35,** Akiyama teaches that the at least one capacitance (Drawing 6, items C1, C2) is directly connected to respective terminals of said first and second transistors (Drawing 6, items TR3, TR4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 2, 16-21, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (Japanese Publication No: 11-194316) in view of Hosokawa et al. (US Patent No: 4,393,380).

34. **As for claim 2,** Akiyama fails to teach that at least the common drive circuit, a display portion and a gate driver circuit for controlling switching of pixels of each line in the display portion are mounted on a substrate, and

35. wherein the common drive circuit is disposed on a position opposite to the gate driver circuit and the display portion therebetween.

36. Hosokawa teaches of at least the common drive circuit (Fig. 4, item 34), a display portion (Fig. 4, items 5, 6, 30, 31) and a gate driver circuit (Fig. 4, item 2) for controlling switching of pixels (Fig. 4, item 5) of each line (Fig. 4, items 32, 33) in the display portion (Fig. 4, items 5, 6, 30, 31) are mounted on a substrate, and

37. wherein the common drive circuit (Fig. 4, item 34) is disposed on a position opposite to the gate driver circuit (Fig. 4, item 2) and the display portion (Fig. 4, items 5, 6, 30, 31) therebetween.

38. All of the component parts are known in Akiyama and Hosokawa. The only difference is the combination of the "old elements" so that the display is between the gate driver circuit and the common drive circuit. Thus, it would have been obvious to one having ordinary skill in the art to have the common drive circuit be positioned position to the gate driver circuit with the display portion in between as taught by Hosokawa with the common drive circuit of Akiyama, since the repositioning of these elements is in no way critically dependent upon the overall operation of the display, and further this configuration could be combined to achieve the predictable result of space and cost efficiency when a display is located in a compact area.

39. **As for independent claim 16,** Akiyama teaches of a display (Drawing 2, item 10) comprising:

40. a substrate (not shown);

41. a display portion (Drawing 2, item 10) integrated on the substrate (not shown); and

42. a gate driver circuit (Drawing 2, item 14) which controls switching of pixels of each line in a display portion (Drawing 2, item 10);

43. a common drive circuit (Drawing 6) for the display portion (Drawing 2, item 10) which simultaneously driving capacitance loads in the display portion (Drawing 2, item 10).

44. Akiyama fails to teach that the common drive circuit is disposed on a position opposite to the gate driver circuit and the display portion therebetween.

45. Hosokawa teaches that the common drive circuit (Fig. 4, item 34) is disposed on a position opposite to the gate driver circuit (Fig. 4, item 2) and the display portion (Fig. 4, items 5, 6, 30, 31) therebetween.

46. All of the component parts are known in Akiyama and Hosokawa. The only difference is the combination of the "old elements" so that the display is between the gate driver circuit and the common drive circuit. Thus, it would have been obvious to one having ordinary skill in the art to have the common drive circuit be positioned position to the gate driver circuit with the display portion in between as taught by Hosokawa with the common drive circuit of Akiyama, since the repositioning of these elements is in no way critically dependent upon the overall operation of the display, and further this configuration could be combined to achieve the predictable result of space and cost efficiency when a display is located in a compact area.

47. **As for claim 17,** Akiyama teaches that the drive circuit (Drawing 6) comprising:

48. a first voltage supply (Drawing 6, item +Vdd) and a second voltage supply (Drawing 6, item –Vee) which respectively supply a high level voltage signal (Drawing 6, item +Vdd) and a low level voltage signal (Drawing 6, item –Vee) to a common electrode;

49. at least one first transistor (Drawing 6, items TR1, TR3) including either a drain or a source terminal connected to the first voltage supply (Drawing 6, item +Vdd);

50. at least one second transistor (Drawing 6, items TR2, TR4) including either a drain or source terminal connected to the second voltage supply (Drawing 6, item –Vee);

51. at least one signal line (Drawing 6, item VCOM) connected to each gate terminal of the first (Drawing 6, items TR1, TR3) and second transistor (Drawing 6, items TR2, TR4); and

52. at least one capacitance load (Drawing 6, items C1, C2) connected to respective terminals of the first (Drawing 6, items TR1, TR3) and the second transistors (Drawing 6, items TR2, TR4) not connected to the first (Drawing 6, item +Vdd) and second voltage supplies (Drawing 6, item -Vee),

53. wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply (Drawing 6, item +Vdd) and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by the second voltage supply (Drawing 6, item –Vee, section [0047]).

54. **As for claim 18,** Akiyama teaches that at least one first transistor comprises P-type transistor (Drawing 6, items TR1, TR3, section [0018]) and the at least one second transistors comprises N-type transistor (Drawing 6, items TR2, TR4, section [0019]), and

55. wherein the gate terminals of the first and second transistors are connected to common signal lines (Drawing 6, items VCOM).

56. **As for claim 21,** Akiyama teaches that the first (Drawing 6, items TR1, TR3) and second transistors (Drawing 6, items TR2, TR4, section [0018]) are comprised of thin-film transistors.

57. **As for claims 30-31,** Akiyama teaches of a level shift circuit (Drawing 2, item 12) connected to the at least one signal line (Drawing 2, items X1-X640x3) and the inversion signal line directly or via a buffer circuit or an inverter circuit (Drawing 2, item 16; Drawing 6).

58. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (Japanese Publication No: 11-194316) in view of Taki (US Publication No: 2002/0000833 A1).

59. **As for claim 4,** Akiyama teaches that the gates of the P-type transistors of the first transistor (Drawing 6, items TR1, TR3) and the N-type transistor of the second transistors (Drawing 6, items TR2, TR4) are connected to one the signal line (Drawing 6, item VCOM).

60. Akiyama fails to teach that the P-type transistors and N-type transistors are connected in parallel to be the first and second transistor, and that the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line.

61. Taki teaches that the P-type transistors and N-type transistors are connected in parallel to be the first and second transistor (Fig. 1b).

62. It would have been obvious to one with ordinary skill in the art at the time the invention was made to connect the P-type transistors and N-type transistors are connected in parallel to be the first and second transistor in order to provide a small area and low-power consumping logic gate cell (Taki, abstract).

63. Taki fails to teach that the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line.

64. Examiner takes official notice that it is well known in the art to have the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line.

65. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line in order to provide a circuit that is most cost and space efficient.

66. **As for claim 5,** Akiyama teaches that a high-level voltage of each signal of the signal line (Drawing 6, item VCOM) and the inversion signal line is a high-level line voltage of the gate driver (Drawing 2, item 14) and

67. wherein a low-level voltage of each signal of the signal line (Drawing 6, item VCOM) and the inversion signal line is a low-level line voltage of the gate driver (Drawing 2, item 14, section [0028]).

68. Claims 19-20, 32, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (Japanese Publication No: 11-194316) in view of Hosokawa et al. (US Patent No: 4,393,380) and Taki (US Publication No: 2002/0000833 A1).

69. **As for claim 19,** Akiyama teaches that the gates of the P-type transistors of the first transistor (Drawing 6, items TR1, TR3) and the N-type transistor of the second transistors (Drawing 6, items TR2, TR4) are connected to one the signal line (Drawing 6, item VCOM).

70. Akiyama fails to teach that the P-type transistors and N-type transistors are connected in parallel to be the first and second transistor, and that the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line.

71. Taki teaches that the P-type transistors and N-type transistors are connected in parallel to be the first and second transistor (Fig. 1b).

72. It would have been obvious to one with ordinary skill in the art at the time the invention was made to connect the P-type transistors and N-type transistors are connected in parallel to be the first and second transistor in order to provide a small area and low-power consuming logic gate cell (Taki, Abstract).

73. Taki fails to teach that the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line.

74. Examiner takes official notice that it is well known in the art to have the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line.

75. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the respective gates of the N-type transistors of the first transistor and the P-type transistors of the second transistor are connected to an inversion signal line of one the signal line in order to provide a circuit that is most cost and space efficient.

76. **As for claim 20,** Akiyama teaches that a high-level voltage of each signal of the signal line (Drawing 6, item VCOM) and the inversion signal line is a high-level line voltage of the gate driver (Drawing 2, item 14) and

77. wherein a low-level voltage of each signal of the signal line (Drawing 6, item VCOM) and the inversion signal line is a low-level line voltage of the gate driver (Drawing 2, item 14, section [0028]).

78. **As for claim 32,** Akiyama teaches of a level shift circuit (Drawing 2, item 12) connected to the at least one signal line (Drawing 2, items X1-X640x3) and the inversion signal line directly or via a buffer circuit or an inverter circuit (Drawing 2, item 16; Drawing 6).

79. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (Japanese Publication No: 11-194316) in view of Taki (U.S. Patent No: 6,329,834 B1).

80. **As for independent claim 34,** in addition to the claim limitations as expressed in claim 1 above, Akiyama fails to teach of at least one first transistor including either a drain or a source terminal directly connected to said first voltage supply;

81. at least one second transistor including either a drain or source terminal directly connected to said second voltage supply.

82. Taki teaches of at least one first transistor (Fig. 19, items 44-45, 49-50) including either a drain or a source terminal directly connected to said first voltage supply (Fig. 19, items Vdd, Gnd);

83. at least one second transistor (Fig. 19, items 44-45, 49-50) including either a drain or source terminal directly connected to said second voltage supply (Fig. 19, items Vdd, Gnd).

84. It would have been obvious to one with ordinary skill in the art at the time the invention was made to arrange the transistors and voltage supplies of Akiyama into the arrangement as specified by Taki in order to provide a small-area and low-power consuming circuit (Taki, column 2, lines 20-25).

Conclusion

85. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

86. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

87. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

88. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

89. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
23 June 2008

Tammy Pham
/Tammy Pham/
Examiner, Art Unit 2629

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629